PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No. 02,957)

IN THE APPLICATION OF:			
Rajamohana Hegde, et al.			
Serial No.	10/603,388	Examiner:	To Be Assigned
Filed:	June 24, 2003	Group Art Unit:	2631
Title:	Method and Apparatus for Delayed Recursion Decoder		

TRANSMITTAL LETTER

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In regard to the above identified application:

1. We are transmitting herewith the attached:

   a. Supplemental Information Disclosure Statement;
   b. Form PTO-1449;
   c. Copy of IDS Citations 10/603,388 (13 references);
   d. Return Receipt Postcard.

2. With respect to additional fees:

   ☒ No additional fee is required.

3. Please charge any additional fees or credit overpayment to Deposit Account No. 13-2490. A duplicate copy of this sheet is enclosed.

4. CERTIFICATE OF MAILING UNDER 37 CFR § 1.8: The undersigned hereby certifies that this Transmittal Letter and the papers, as described in paragraph 1 hereinabove, are being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on this 20th day of November, 2003.

By: _____
Robert J. Irvine
Reg. No. 41,865

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Pursuant to the duty of disclosure provided by 35 C.F.R. § 1.56 and §§ 1.97-98, the applicants wish to make the following references of record in the above-identified application. Copies of the references are enclosed. Copies are also listed in the PTO-1449 form enclosed herewith. It is requested that the documents be given careful consideration and that they be cited of record in the prosecution history of the present application so that they will appear on the face of the patent issuing from the present application.

Portions of the references may be material to the examination of the pending claims, however no such admission is intended. 37 C.F.R. 1.97 (h). The references have not been reviewed in sufficient detail to make any other representation and, in particular, no representation is intended as to the relative importance of any portion of the references. This Statement is not a representation that the cited references have effective

dates early enough to be "prior art" within the meaning of 35 U.S.C. sections 102 or 103, nor is this submission to be construed as a representation that a search has been made.

CITED REFERENCES

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

1. Erik Paaske and Jakob Dahl Andersen, "High Speed Viterbi Decoder Architecture", - First ESA Workshop on Tracking, Telemetry and Command Systems, ESTEC, June 1998.
2. Chinnery, D. G., and Keutzer, K., "Achieving 550 MHz in an ASIC Methodology", Proceedings of the 38th Design Automation Conference, Las Vegas, NV, Pages 420-425, June 2001.
3. McGinty, Nigel C.; Kennedy, Rodney A.; and Hoeher, Peter, "Equalization of Sparse ISI Channels Using Parallel Trellises", Proceedings, GLOBECOM'98, November, 1998.
4. Liu, K. J. Ray and Raghupathy, Arun, "Algorithm-Based Low-Power and High-Performance Multimedia Signal Processing", Proceedings of the IEEE, Volume 86, No. 6, June 1998.
5. Kang, Inyup and Willson, Alan N. Jr., "Low-Power Viterbi Decoder for CDMA Mobile Terminals", IEEE Journal of Solid-State Circuits, Volume 33, No. 3, March 1998.
6. Furuya, Yukitsuna; Akashi, Fumio and Murakami, Shuji, "A Practical Approach Towerad Maximum Likelihood Sequence Estimation for Band-Limited Nonlinear Channels", IEEE Transactions on Communications, Volume Com-31, No. 2, February, 1983.
7. Summerfield, S., "Analysis of Convolutional Encoders and Synthesis of Rate-2/n Viterbi Decoders", IEEE Transaction on Information Theory, Volume 42, Number 4, Page 1280, July 1996.
8. Choi, Young-bae, "A VLSI Architecture for High Speed and Variable Code Rate Viterbi Decoder" ICSPAT, Proceedings, Pages 1918-22, 2000.
9. Reeve, J.S., "A Parallel Viterbi Decoding Algorithm", July 21, 2000.
10. Gross, Warren J.; Gaudet, Vincent C. and Gulak, P. Glenn, "Difference Metric Soft-Output Detection: Architecture and Implementation", IEEE Transactions on Circuits and Systems II (Analog and Digital Signal Processing), Volume 48, No. 10, Pages 904-911, October 2001.
11. Ranpara, Samirkumar, "A Low-Power Viterbi Decoder Design for Wireless Communications Applications", Int. ASIC Conference, September 1999.
12. Boo, M.; Arguello, F. ; Bruguera, J.D.; and Zapata, E.L., "High-Speed Viterbi Decoder: An Efficient Scheduling Method to Exploit the Pipelining", IEEE Int'l. August 19-21, 1996.

13. Chinnery, David, Nikolic, Borivoje and Keutzer, Kurt, "Achieving 550 MHz in an ASIC Methodology", Presentation, Proceedings of the 38th Design Automation Conference, Las Vegas, NV, pp. 420-425, June 2001.

Respectfully submitted,
McDonnell Boehnen Hulbert & Berghoff

Date: November 20, 2003

By: _____
Robert J. Irvine
Registration No. 41,865

Form PTO-1449 (modified)	Atty. Docket No. 02-957	Serial No. 10/603,388
List of Patents and Publications for Applicant's SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	Applicant Rajamohana Hegde, et al.	
(Use several sheets if necessary)	Filing Date: June 24, 2003	Group: 2631

U.S. Patent Documents	Foreign Patent Documents	Other Art
None	*None*	*See Page 1 and 2*

Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C6	Furuya, Yukitsuna; Akashi, Fumio and Murakami, Shuji, "A Practical Approach Towerad Maximum Likelihood Sequence Estimation for Band-Limited Nonlinear Channels", IEEE Transactions on Communications, Volume Com-31, No. 2, February, 1983.
	C7	Summerfield, S., "Analysis of Convolutional Encoders and Synthesis of Rate-2/n Viterbi Decoders", IEEE Transaction on Information Theory, Volume 42, Number 4, Page 1280, July 1996.
	C8	Choi, Young-bae, "A VLSI Architecture for High Speed and Variable Code Rate Viterbi Decoder" ICSPAT, Proceedings, Pages 1918-22, 2000.
	C9	Reeve, J.S., "A Parallel Viterbi Decoding Algorithm", July 21, 2000.
	C10	Gross, Warren J.; Gaudet, Vincent C. and Gulak, P. Glenn, "Difference Metric Soft-Output Detection: Architecture and Implementation", IEEE Transactions on Circuits and Systems II (Analog and Digital Signal Processing), Volume 48, No. 10, Pages 904-911, October 2001.
	C11	Ranpara, Samirkumar, "A Low-Power Viterbi Decoder Design for Wireless Communications Applications", Int. ASIC Conference, September 1999.
	C12	Boo, M.; Arguello, F. ; Bruguera, J.D.; and Zapata, E.L., "High-Speed Viterbi Decoder: An Efficient Scheduling Method to Exploit the Pipelining", IEEE Int'l. August 19-21, 1996.
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(Use several sheets if necessary)	**Filing Date:** June 24, 2003	**Group:** 2631

U.S. Patent Documents	Foreign Patent Documents	Other Art
None	*None*	*See Page 1*

U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1						
	A2						

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						
	B2						

Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	Erik Paaske and Jakob Dahl Andersen, "High Speed Viterbi Decoder Architecture", - First ESA Workshop on Tracking, Telemetry and Command Systems, ESTEC, June 1998.
	C2	Chinnery, D. G., and Keutzer, K., "Achieving 550 MHz in an ASIC Methodology", Proceedings of the 38th Design Automation Conference, Las Vegas, NV, Pages 420-425, June 2001.
	C3	McGinty, Nigel C.; Kennedy, Rodney A.; and Hoeher, Peter, "Equalization of Sparse ISI Channels Using Parallel Trellises", Proceedings, GLOBECOM'98, November, 1998.
	C4	Liu, K. J. Ray and Raghupathy, Arun, "Algorithm-Based Low-Power and High-Performance Multimedia Signal Processing", Proceedings of the IEEE, Volume 86, No. 6, June 1998.
	C5	Kang, Inyup and Willson, Alan N. Jr., "Low-Power Viterbi Decoder for CDMA Mobile Terminals", IEEE Journal of Solid-State Circuits, Volume 33, No. 3, March 1998.

EXAMINER:	DATE CONSIDERED:

EXAMINER: INITIAL IF REFERENCE CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED. INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.